AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of suppressing sub-threshold leakage in a transistor of an integrated circuit, the method comprising:

storing a value in a memory cell coupled to a gate of the transistor; and

applying a gate to source voltage to the transistor that under-drives the transistor.

2. (Currently Amended) The method of Claim 1, wherein if the transistor is an NMOS device, then applying includes:

providing a slightly negative voltage from the memory cell to [[a]] the gate of the transistor.

3. (Original) The method of Claim 2, wherein the slightly negative voltage is between 0 and approximately –0.2 V.

4. (Original) The method of Claim 2, wherein the slightly negative voltage is approximately –0.1 V.

5. (Currently Amended) The method of Claim 1, wherein if the transistor is an NMOS device, then applying includes:

providing a first voltage from the memory cell to [[a]] the gate of the transistor,

wherein the first voltage is slightly less than a second voltage provided to a source of the transistor.

6. (Original) The method of Claim 1, wherein if the transistor is an NMOS device having a gate voltage of 0 V, then applying includes:

providing a slightly positive voltage to a source of the transistor.

7. (Original) The method of Claim 6, wherein the slightly positive voltage is between 0 and approximately 0.2 V.

8. (Original) The method of Claim 6, wherein the slightly positive voltage is approximately 0.1 V.

9. (Currently Amended) The method of Claim 1, wherein if the transistor is an NMOS device, then applying includes:

providing a first voltage to a source of the transistor,

wherein the first voltage is slightly greater than a second voltage provided from the memory cell to [[a]] the gate of the transistor.

10. (Currently Amended) The method of Claim 1, wherein if the transistor is a PMOS device having a source voltage of VDD, then applying includes:

providing a slightly more positive voltage than VDD from the memory cell to [[a]] the gate of the transistor.

11. (Original) The method of Claim 10, wherein the slightly more positive voltage is VDD + N, wherein $0 < N \leq 0.2$ V.

12. (Original) The method of Claim 10, wherein the slightly negative voltage is approximately VDD + 0.1 V.

13. (Currently Amended) The method of Claim 1, wherein if the transistor is a PMOS device, then applying includes:

providing a first voltage from the memory cell to [[a]] the gate of the transistor,

wherein the first voltage is slightly greater than a second voltage provided to a source of the transistor.

14. (Original) The method of Claim 1, wherein if the transistor is a PMOS device having a gate voltage of VDD, then applying includes:

providing a slightly less positive voltage than VDD to a source of the transistor.

15. (Original) The method of Claim 14, wherein the slightly less positive voltage is VDD - N, wherein $0 < N \leq 0.2$ V.

16. (Original) The method of Claim 14, wherein the slightly positive voltage is approximately VDD - 0.1 V.

17. (Currently Amended) The method of Claim 1, wherein if the transistor is a PMOS device, then applying includes:

providing a first voltage to a source of the transistor,

wherein the first voltage is slightly less than a second voltage provided from the memory cell to [[a]] the gate of the transistor.

18. (Original) The method of Claim 1, wherein applying includes:

providing a level shifter that receives a logic signal from the integrated circuit and generates a modified gate voltage for the transistor,

wherein the modified gate voltage is one of:

slightly less than a source voltage of the transistor, if the transistor is an NMOS device, and

slightly greater than a source voltage of the transistor, if the transistor is a PMOS device.

19. (Original) A memory cell for suppressing sub-threshold leakage in a transistor, the memory cell comprising:

a plurality of transistors configurable to store a value,

wherein the value can under-drive the transistor in its off state.

20. (Original) The memory cell of Claim 19, wherein if the transistor is an NMOS device having a source voltage of VSS and the memory cell drives a gate of the transistor, then the value is slightly more negative than VSS.

21. (Original) The memory cell of Claim 19, wherein if the transistor is an PMOS device having a source voltage of VDD and the memory cell drives a gate of the transistor, then the value is slightly more positive than VDD.

22. (Original) The memory cell of Claim 19, wherein if the transistor is an NMOS device having a gate voltage of VSS and the memory cell drives a source of the transistor, then the value is slightly more positive than VSS.

23. (Original) The memory cell of Claim 19, wherein if the transistor is an PMOS device having a gate voltage of VDD and the memory cell drives a source of the transistor, then the value is slightly less than VDD.

24. (Original) A level shifter that receives a non-memory signal and generates a modified gate voltage for a transistor, the modified gate voltage able to suppress sub-threshold leakage in a transistor, the level shifter comprising:

means for generating slightly less than a source voltage of the transistor for the modified gate voltage, if the transistor is an NMOS device; and

means for generating slightly greater than a source voltage of the transistor for the modified gate voltage, if the transistor is a PMOS device.

25. (Original) A structure for suppressing sub-threshold leakage in a transistor, the structure comprising:

a circuit that creates a negative gate to source voltage when the transistor is in its off state.